Comp 120 Syllabus  
Spring Semester 2005


Schedule:

1. (1/13) Course Introduction and Information Theory (not in book)  
2. (1/18) Information Encoding and Representations (not in book)  
3. (1/20) Processing Information with Transistors (not in book)  
4. (1/25) Boolean Gates and Combinational Logic (Appendix B.1-B.3)  
5. (1/27) Latches, Memory, and Registers (Appendix B.5)  
6. (2/1) Synchronous Logic (Appendix B.4, B.7)  
7. (2/3) Finite State Machines (Appendix B.6)  
8. (2/8) Pipelining Combinational Circuits (Chapter 6.1)  
9. (2/10) Arithmetic Circuits (Chapter 4)  
10. (2/15) Review  
11. (2/17) Quiz #1  
12. (2/22) Programmable Machines (not in book)  
13. (2/24) Instruction Set Design (Chapter 3)  
14. (3/1) Building a Computer (Chapter 5.1-5.3)  
15. (3/3) Assemblers and Compilers (Appendix A.1-A5)  
17. (3/10) Computer Performance (Chapter 2, Chapter 5.4-5.5)  
18. (3/22) CPU Pipelining – Part 1 (Chapter 6)  
19. (3/24) CPU Pipelining – Part 2 (Chapter 6)  
20. (3/29) Review  
21. (3/31) Quiz #2  
22. (4/5) Memory Hierarchy (Chapter 7.1)  
23. (4/7) Cache Principles (Chapter 7.2)  
24. (4/12) Cache Structures (Chapter 7.3)  
25. (4/14) Virtual Memory (Chapter 7.4-7.11)  
26. (4/19) System Interconnect (Chapter 8)  
27. (4/21) Virtual Machines and Kernels (not in book)  
28. (4/26) Multiprocessors and Parallel Computers (Chapter 9)  
29. (4/28) Review

(5/10) Final Exam 9:00-12:00

Grading:

Best 8 scores out of 10 Problem Sets (5% each) 40%  
2 in-class quizzes (15% each) 30%  
Final Exam 30%

Problem sets will be distributed on Thursdays and are due back on the next Thursday class meeting (before the beginning of lecture). This means, you will have at least one and sometimes two weeks to complete each set. No problem set will be due the week of a quiz. Late problem sets will not be accepted, but the lowest two problem-set scores will be dropped.