

Comp 120 Computer Organization

Spring 2005

Problem Set #2

Issued Thursday, 1/27/05; Due Thursday, 2/03/05

Homework Information: Some of the problems are probably too long to be done the night before the due date, so plan accordingly. Late homework will not be accepted. Feel free to get help from others, but the work you hand in should be your own.

Problem 1. “Being Combinational”

In lecture 3, you learned two basic principles regarding the class of *combinational devices*. The first allows us to build a combinational device from, e.g., electronic components:

A *combinational device* is a circuit element that has

- one or more digital inputs
- one or more digital outputs
- a functional specification that details the value of each output for every possible combination of valid input values
- a timing specification consisting (at minimum) of an upper bound t_{pd} on the required time for the device to compute the specified output values from an arbitrary set of stable, valid input values

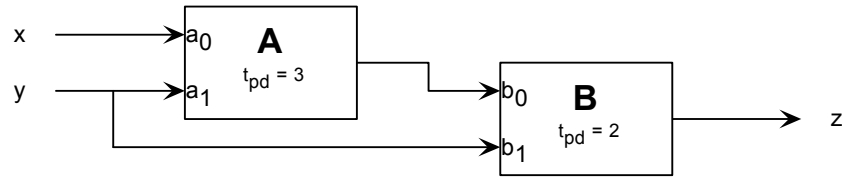
while the second allows us to construct complex combinational devices from acyclic circuits containing simpler ones:

A set of interconnected elements is a combinational device if

- each circuit element is combinational
- every input is connected to exactly one output or to some vast supply of 0's and 1's
- the circuit contains no directed cycles

In this problem, you are asked you to think carefully about why these rules work – in particular, why an acyclic circuit of combinational devices, constructed according to the second principle, is itself a combinational device as defined by the first. You may assume for the following that every input and output is a logical 0 or 1.

Consider the following 2-input acyclic circuit whose two components, A and B, are each combinational devices:



The propagation delay – the upper bound on the output settling time – for each device is specified in nanoseconds. The functional specifications for each component are given as truth tables detailing output values for each combination of inputs:

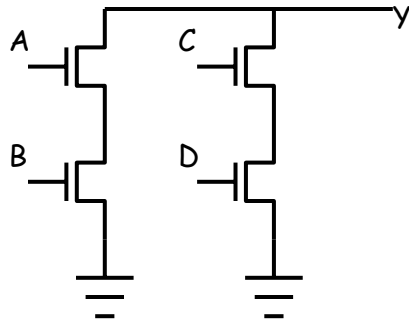
a_0	a_1	A (a_0, a_1)	b_0	b_1	B (a_0, a_1)
0	0	1	0	0	0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	1	1	1

- (A) Give a truth table for the acyclic circuit, i.e. a table that specifies the value of z for each of the possible combinations of input values on x and y .
- (B) Describe a general procedure by which a truth table can be computed for each output of an *arbitrary* acyclic circuit containing only combinational components. [*HINT*: add a functional specification to each circuit node].
- (C) Specify a propagation delay (the upper bound required for each combinational device) for the circuit.
- (D) Describe a general procedure by which a propagation delay can be computed for an arbitrary acyclic circuit containing only combinational components. [*HINT*: add a timing specification to each circuit node].
- (E) Do your general procedures for computing functional specifications and propagation delays work if the restriction to acyclic circuits is relaxed? Explain.

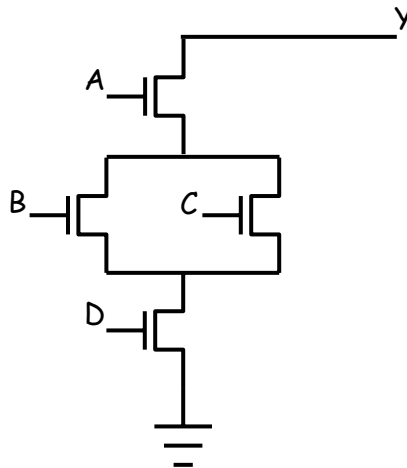
Problem 2. “Fishing for Complements”

Show the complementary set of p-channel or n-channel transistors that complete the following CMOS circuits:

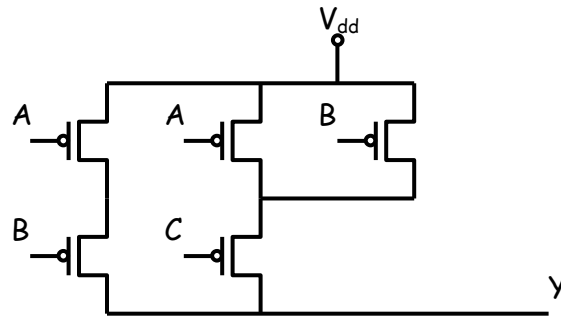
a)



b)

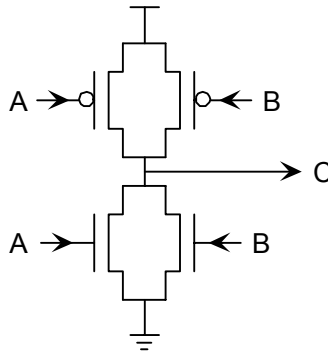


c)



Problem 3. “Illogical Conclusions”

Bud Leville, a circuit designer who missed several early Comp 120 lectures, is struggling to design his first CMOS logic gate. He has implemented the following circuit:



Bud has fabricated 100 test chips containing this circuit, and has a simple testing circuit which allows him to try out his proposed gate statically for various combinations of the A and B inputs. He has burned out 97 of his chips, and needs your help before destroying the remaining three. He is certain he is applying only valid input voltages, and expects to find a valid output at terminal C. Bud also keeps noticing a very faint smell of smoke.

- (A) What is burning out Bud’s test chips? Give a specific scenario, including input values together with a description of the failure scenario. For what input combinations will this failure occur?
- (B) Are there input combinations for which Bud can expect a valid output at C? Explain.

One of Bud’s test chips has failed by burning out the pullup connected to A as well as the pulldown connected to B. Each of the burned out FETs appears as an open circuit, but the rest of the circuit remains functional.

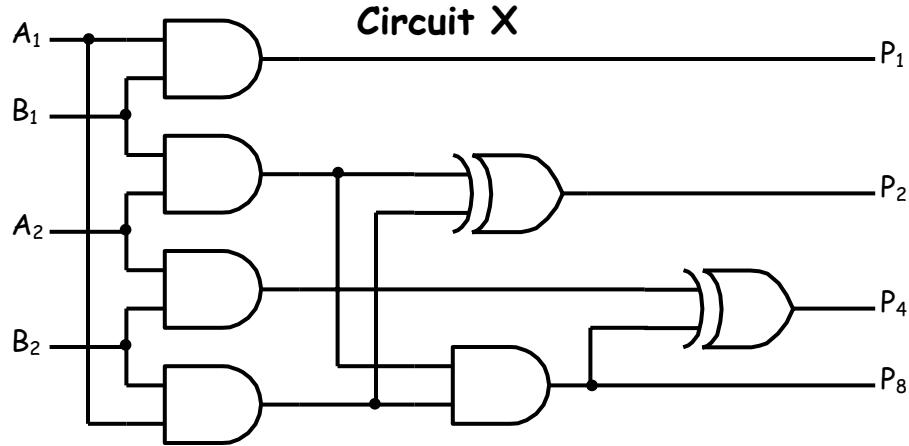
- (C) Can the resulting circuit be used as a combinational device? Explain its behavior for each combination of valid inputs.

In order to salvage his remaining three chips, Bud connects the A and B inputs of each and tries to use it as a single-input gate.

- (D) Can the result be used as a single-input combinational device? Explain.

Problem 4. “Go Forth and Multiply”

- a) Design logic to perform the multiplication of two-2-bit unsigned integers producing a 4-bit result (Hint: use a separate Karnaugh map for each output bit). Draw a gate-level-circuit diagram and give the number of gates needed to build the resulting circuit (Count 3-input and 4-input gates as a single gate).
- b) Determine the function of the following circuit by writing out and examining its truth table.



- c) What aspects of minimization does a minimal sum-of-products realization not consider?

For Circuit X assume that AND gates have a propagation of 2 nS and a contamination delay of 1nS, while XOR gates have a propagation delay of 3 nS and contamination delay of 2 nS.

- d) Compute the aggregate contamination and propagation delays for Circuit X. What is the maximum frequency that the inputs of Circuit X be changed while insuring that all outputs are stable for 5 nS?
- e) Suppose the gates below are added to Circuit X, how are the answers to part d) affected?

