

Comp 120 Computer Organization
Spring 2005

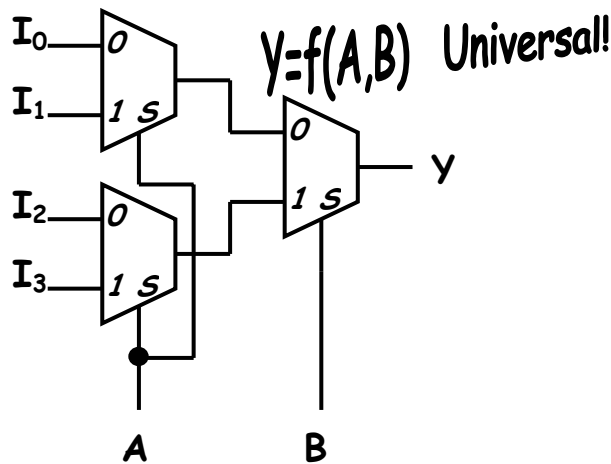
Problem Set #3

Issued Thursday, 2/3/05; Due Thursday, 2/10/05

Homework Information: Some of the problems are probably too long to be done the night before the due date, so plan accordingly. Late homework will not be accepted. Feel free to get help from others, but the work you hand in should be your own.

Problem 1. “Mux Madness”

During a particularly boring Comp 120 lecture, Lee Hart found himself dosing off in the middle of a discussion about the universality of NAND and NOR gates. When, in a dream, he suddenly realized that multiplexers are also universal. At the close of lecture he awakes and jots the following diagram on the back of his problem set:



Help explain Lee’s insight.

- A) Give binary values for I_0 , I_1 , I_2 , and I_3 which implement the following functions on the two inputs A and B : AND(A,B), OR(A,B), XOR(A,B), NAND(A,B), and NOR(A,B).
- B) Can any 2-input Boolean function be implemented using Lee’s structure? Explain why or why not.

Later, in an effort to impress his TA, Lee shows up at his office hours to explain his discovery. He decides to make his point by constructing several standard gates using his universal structure. So he drags out his nifty bag of parts only to discover that he has only two 2-input multiplexers. Then suddenly it dawned on him; assuming he had a source for the logical constants “0” and “1”, he could build every 2-input gate using only 2 multiplexers.

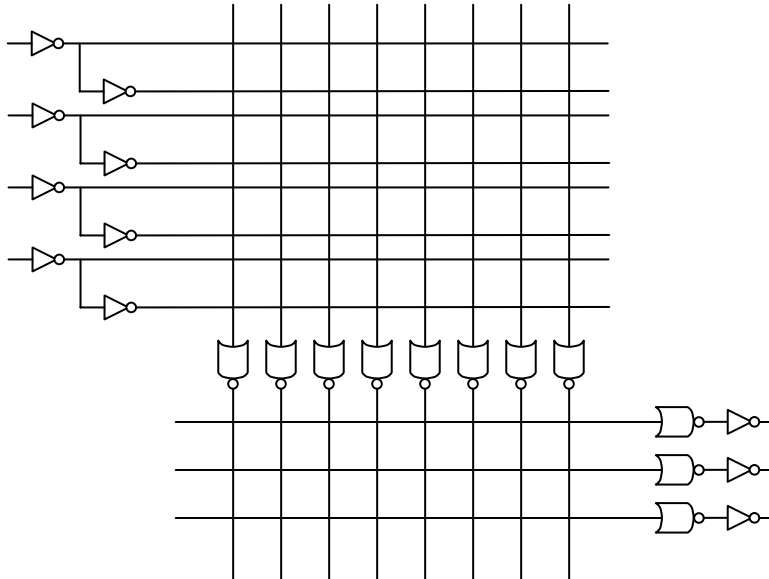
- C) Show how Lee can implement an inverter, as well as every 2-input gate using no more than 2-multiplexers to construct each one.

Problem 2. “Assigning Priorities”

A common logic block known as a 4-input *priority encoder* has the truth table shown below:

I ₃	I ₂	I ₁	I ₀	A ₁	A ₀	E
1	X	X	X	1	1	1
0	1	X	X	1	0	1
0	0	1	X	0	1	1
0	0	0	1	0	0	1
0	0	0	0	0	0	0

- A) Write out a table containing the entries for a ROM implementation of the priority encoder described. How many words does the ROM have? How many bits?
- B) Reimplement the 4-input priority encoder described above using a PLA. A common technique for depicting schematic PLAs is shown below:

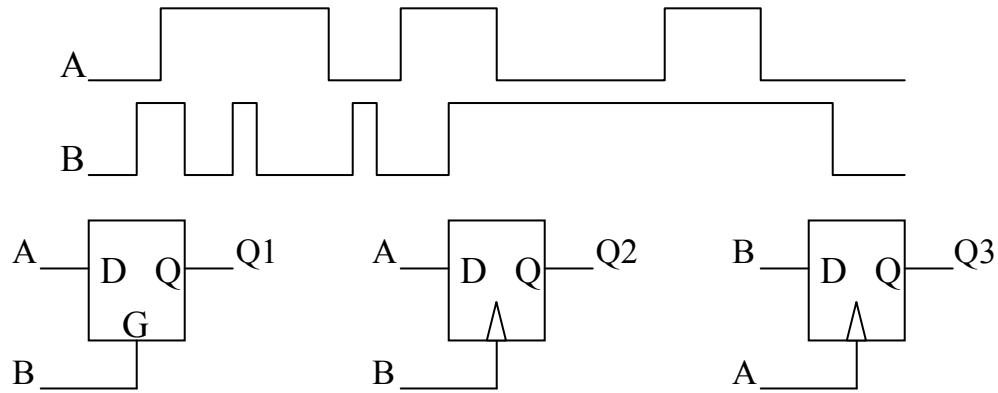


Placing an X at the intersection of a pair of wires in either array indicates a unique connection to the associated NOR gate. It is also helpful to label each WORD-line with its corresponding product term across the bottom of the figure.

- C) Design a 2-bit priority encoder using standard logic gates. Then design a 4-input priority encoder that uses your 2-bit design as a building block.
- D) Discuss the relative merits and disadvantages of your three designs. Consider the ease of design, number of components used, and the likely propagation delays of each approach.

Problem 3. “Getting Faint Memories to Register”

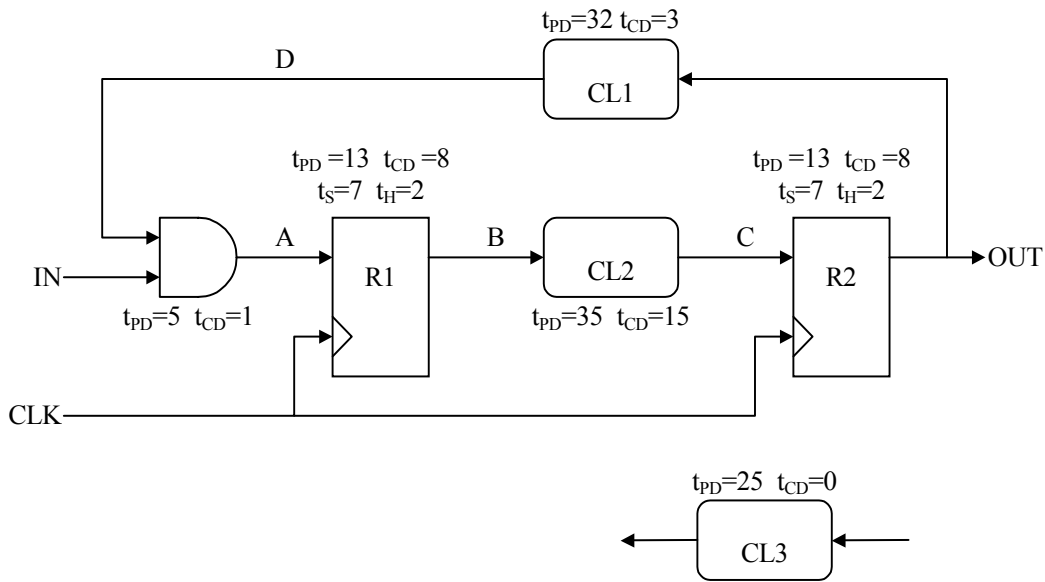
- A) Given the following sequences A and B, draw the timing diagrams for the outputs Q1, Q2, and Q3. Assume setup and hold times are met in all cases and that the propagation delay is negligible. Also, assume a low signal as the initial value for Q1, Q2, and Q3.



- B) Design a falling or negative-edge triggered flip-flop using two latches. Then draw the timing diagram for your flip-flop in response to connecting the A timing sequence from above to the D input and the B timing sequence to the clock.

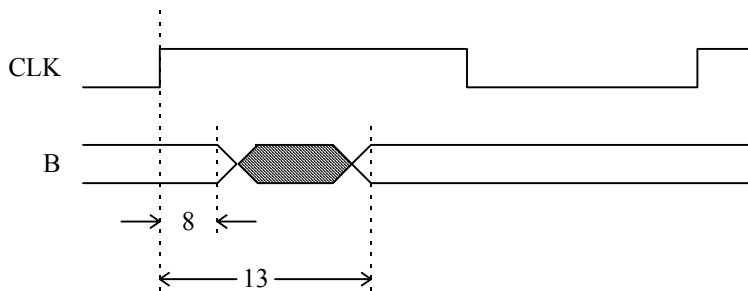
Problem 4. “Synchronous Circuit Circus”

Consider the following circuit:



CL1, CL2 and CL3 represent combinational logic circuits with the timing parameters indicated. R1 and R2 are rising edge-triggered flip-flops. All delays are in nanoseconds.

- (A) Add the signals A, C, OUT and D to the timing diagram show below. Be sure to indicate the times when signals start to change and when they become stable.



- (B) What is the maximum frequency for CLK that still guarantees that the circuit will operate correctly? Explain your calculation and indicate which path through the circuit that determines the maximum frequency.
- (C) Suppose CL1 is now replaced by CL3. Calculate the new maximum frequency for CLK and indicate the critical path.
- (D) What timing constraints must be placed on the IN signal to ensure correct operation? Explain your reasoning and draw a timing diagram that shows your constraints.